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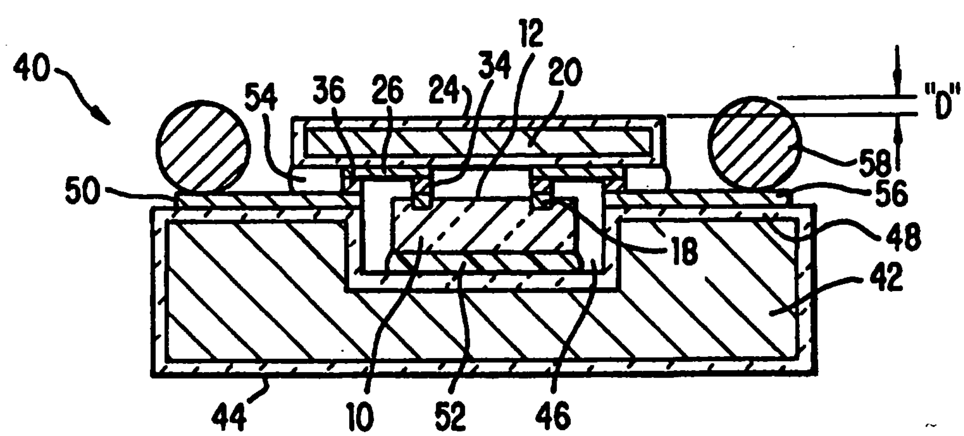

(57) Abstract

There is provided a metallic component (20) for an electronic package (40). The component (20) is coated with an electrically non-conductive layer (24) and has a plurality of conductive circuit traces (26) on a surface. The circuit traces (26) are soldered (34) directly to the input/output pads (18) of an integrated circuit device (10) and to a second plurality of circuit traces (50). The component (20) may include a heat sink to enhance dissipation of heat from the encapsulated integrated circuit device (10).

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COMPONENTS FOR HOUSING AN INTEGRATED CIRCUIT DEVICE

This invention relates to components for electronic packages. More particularly, there are provided metallic substrates and heat sinks useful in ball grid array electronic packages.

Microelectronic devices are typically manufactured from a semiconductor material such as silicon, germanium or gallium/arsenide. The semiconductor material is fashioned into a die, a generally rectangular structure having circuitry formed on one surface. Along the periphery of that electrically active surface are input/output pads to facilitate electrical interconnection to external circuitry.

The semiconductor device is brittle and requires protection from moisture and mechanical damage. This protection is provided by an electronic package. The electronic package further contains an electrically conductive means to transport electrical signals between the semiconductor device and the external circuitry.

One electronic package is disclosed in U.S. Patent No. 4,939,316 to Mahulikar et al. The patent discloses separate anodized aluminum or aluminum alloy base and cover components defining a cavity. A leadframe is disposed between the base and the cover and adhesively bonded to both. A semiconductor device is encased within the cavity and electrically interconnected to the inner lead ends of the leadframe. The outer lead ends of the leadframe extend beyond the package perimeter and are interconnected to external circuitry.

The available space on a printed circuit board is limited and it is desirable to minimize the peripheral area of a package. The peripheral area of a leaded package extends beyond the perimeter of the package base and cover to a point defined by the outer lead portions of the leadframe.

To minimize the peripheral area of an electronic package, electrical interconnection may be through a package component as disclosed in PCT International Application No. PCT/US94/02113 that was published on September 29, 1994. The ball grid array package has a metallic base coated with an electrically non-conductive layer. Conductive vias extend through apertures formed through the base. One end of the via is electrically interconnected to the semiconductor device and the other end is bonded to a solder ball for attachment to external circuitry.

In PCT International Application No. PCT/US95/08305, ball grid array electronic packages are disclosed that do not require vias extending through a metallic substrate. The metallic substrate is coated with an electrically non-conductive layer and circuit traces are formed on this electrically non-conductive layer to electrically interconnect a semiconductor device to external solder balls.

While the ball grid array electronic packages disclosed in the above patent applications have proven satisfactory, the inventors have developed electronic package components that improve the electrical properties, the thermal characteristics and the reliability of the package.

Accordingly, it is an object of the present invention to provide components for an electronic package that improve the electrical performance of the package, the thermal performance of the package and the package reliability.

It is a feature of the invention that in one embodiment, electrically conductive circuit traces are formed on a component of the package and directly interconnect input/output pads of an integrated circuit device to external circuitry. In a second embodiment of the invention, both the base component and the cover component include a seal ring bondable to a hermetic sealant. In yet another embodiment of the invention, the component includes an integral heat sink to improve thermal dissipation or the heat sink has a central channel to receive a thermal fluid.

Among the advantages of the invention are that the electronic packages do not require wire bonds and are not subject to device failure due to breakage of the wire bonds. Another advantage is that the package components are suitable for hermetic sealing to enhance reliability. Another advantage of the invention is a heat sink to improve thermal dissipation.

In accordance with the invention, there is provided a component for an electronic package having a metallic substrate coated with an electrically non-conductive layer. A first plurality of conductive circuit traces are formed on a surface of the component. The circuit traces are adapted to be bonded directly to the input/output pads of an integrated circuit device and bonded such

as by soldering to a second plurality of circuit traces.

In a second embodiment of the invention, there is provided a component for an electronic package having a metallic substrate coated with a first electrically non-conductive layer. A first plurality of conductive circuit traces are formed on a peripheral surface of this component with a second electrically non-conductive layer formed about the periphery of the component overlying the mid-portion of the circuit traces.

In yet another embodiment of the invention, there is provided a component for an electronic package. This package includes a metallic substrate having first and second opposing surfaces. An integrated circuit device is bonded directly to the first surface and either a plurality of protrusions extend from the periphery of the second surface of the substrate with a central portion of the second surface essentially free of protrusions or a plurality of protrusions extend outward from the center of this second surface and run generally parallel to the second surface.

In yet another embodiment of the invention, there is provided a base component and a cover component bonded together to define a cavity. A portion of this cavity is occupied by an integrated circuit device. Essentially the remainder of the cavity is filled with a thermally conductive, electrically non-conductive fluid. At least one aperture formed in either the base component or the cover component communicates this fluid to an

internal channel of a heat sink bonded to the aperture containing component.

The above stated objects, features and advantages will become more apparent from the specification and drawings that follow.

Figure 1 shows in top planar view a cover component for an electronic package in accordance with the present invention.

Figure 2 shows in cross-sectional representation the cover component of Figure 1.

Figure 3 shows in cross-sectional representation the cover component of Figure 1 and Figure 2 incorporated into a ball grid array package.

Figure 4 shows in cross-sectional representation another embodiment of the cover component of Figure 1 and Figure 2.

Figure 5 shows in cross-sectional representation an electronic package component for a hermetic ball grid array package.

Figure 6 shows in top planar view the component of Figure 5.

Figure 7 shows in cross-sectional representation another component for a hermetic ball grid array package.

Figure 8 shows in top planar view the hermetic ball grid array package component of Figure 7.

Figure 9 shows in cross-sectional representation a hermetic array package.

Figure 10 shows in cross-sectional representation a hermetic package having side terminal pins.

Figure 11 shows a base component for an electronic package having an integral heat sink.

Figure 12 shows in top planar view the integral heat sink of Figure 11.

Figure 13 shows in cross-sectional representation a base component having another integral heat sink.

Figure 14 shows in top planar view the integral heat sink of Figure 13.

Figure 15 shows in cross-sectional representation a thermal fluid containing heat sink for use with an electronic package.

Figure 16 shows in cross-sectional representation another thermal fluid containing heat sink in accordance with the invention.

Figure 17 illustrates an integrated circuit device as known from the prior art.

Figure 18 illustrates in cross sectional representation the component of Figure 1 used to support a plurality of integrated circuit devices.

Figure 19 illustrates in cross sectional representation a second embodiment in which the component of Figure 1 is used to support a plurality of integrated circuit devices.

Figure 20 illustrates in cross sectional representation thermal coupling of the component of Figure 1 to an external heat sink.

Figure 21 shows in cross sectional representation electrical coupling of an integrated circuit device to a ball grid array electronic package.

Figure 22 shows in top planar view the integral heat sink of Figure 11 with protrusions extending across the central portion.

Figure 17 illustrates an integrated circuit device 10 as known from the prior art. Also known as a semiconductor chip or semiconductor die, the integrated circuit device 10 has a front side 12 and an opposing back side 14. The integrated circuit device 10 is formed from a semiconductor material such as silicon, germanium or gallium/arsenide. By selectively doping portions of the front side 12 with other materials, circuitry 16, that is only partially illustrated in Figure 17, is formed in the front side. The circuitry 16 terminates at metallized input/output (I/O) pads 18. The metallization is selected to facilitate electrical interconnection of the I/O pads 18 to external circuitry. For example, if wire bonds are to be attached by thermal compression bonding, the metallization may be aluminum. If the I/O pads 18 are to be directly soldered to a substrate as in flip chip or C4 (controlled collapse chip connection), the metallization may be palladium.

The opposing back side 14 of the integrated circuit device 10 is usually the semiconductor material or a metallization such as nickel or gold.

Figure 1 illustrates in top planar view a component 20 for an electronic package that is bonded directly to the I/O pads of an integrated circuit device. The component 20 is illustrated in cross-section in Figure 2. Throughout this patent application, the "major surfaces" refer to those illustrated in Figure 1, that is the length and

width of the various components. The perpendicular sides corresponding to Figure 2 are not considered a "major surface".

Referring to both Figure 1 and Figure 2, the component 20 has a substrate 22 formed from any material having a coefficient of thermal expansion between that of silicon ($50x10^{-7}/°C$) and that of aluminum ($240x10^{-7}/°C$). When the substrate 22 is metallic, the substrate is coated with an electrically non-conductive layer 24. By metallic, it is meant that the substrate 22 is a metal, metal alloy, metal based composite or metal based compound and generally considered to be electrically conductive. Suitable materials for the metallic substrate include copper, aluminum, iron, nickel, molybdenum and alloys thereof. Copper, aluminum and alloys thereof are preferred due to high thermal conductivity. Aluminum alloys are most preferred due to the added advantage of light weight.

Suitable clads for the substrate 22 include copper/invar/copper and copper/molybdenum/copper. The thickness of each cladding layer and the cladding core is selected to achieve a composite having a desired coefficient of thermal expansion and a desired coefficient of thermal conductivity.

Suitable non-metals for the substrate 22 include ceramics such as aluminum oxide, aluminum nitride, silicon carbide, and composites thereof and glasses such as borosilicates.

When the metallic substrate 22 is aluminum or an aluminum based alloy, the non-conductive layer 24 is typically an anodic film. The anodic film 24 is from about 0.013 millimeter to about 0.076 mm

(0.0005-0.003 inch) and typically from about 0.013 mm to about 0.05 mm (0.0005-0.002 inch) to electrically isolate circuitry without significantly reducing thermal conductivity.

When the metallic substrate is a metal that is not anodizable, the non-conductive layer 24 may be an oxide, nitride or carbide layer. These layers are readily formed by heating in an effective gaseous atmosphere, by chemical vapor deposition or physical vapor deposition. Alternatively, the non-conductive layer 24 may be a thin layer of a polymer or a glass. Flexible polymers such as polyimides, modified epoxies and silicones that flow when stressed are particularly preferred. These materials compensate for coefficient of thermal expansion differences between the electronic package and the surface to which that package is mounted thereby improving the reliability of the mounting.

A first plurality of conductive circuit traces 26 is formed on a first surface 28 of the metallic substrate 22. While the first plurality of conductive circuit traces 26 may be formed on the first surface 28 by any desired means, including lamination or adhesive bonding, it is preferred that the circuit traces 26 be in direct contact with the non-conductive layer 24 and be formed by a process such as chemical vapor deposition, physical vapor deposition, electroless plating or electrolytic plating.

The circuit traces 26 have an interior termination end 30 and an exterior termination end 32 and are formed from an electrically conductive

material or combination of materials and are predominantly copper or a copper alloy.

The interior termination ends 30 are adapted to be soldered directly to the I/O pads of an integrated circuit device and are in a pattern aligned with those I/O pads. A first bump 34 may be deposited on the interior termination ends 30. Typically, the first bump will be a low melting alloy such as a lead/tin alloy, although an electrically conductive adhesive or an electrically conductive solder glass may also be utilized. Alternatively, the first solder bump may be deposited on the I/O pads of the integrated circuit device.

The solder need not be homogeneous. Alternatives for the first solder bumps 34 include solder covered metallic spheres, such as solder coated copper balls. The first solder bumps may be gold or another material built up on the I/O pads 18 by a process such as evaporation, sputtering, plating or wire bumping. In wire bumping, a metallic wire, typically gold, aluminum or an alloy thereof, is thermocompression or thermosonically bonded to the I/O pad forming a bond ball with a wire tail extending therefrom. The wire tail is subsequently removed. Conductive adhesives such as a silver powder filled epoxy can also be used.

Second solder bumps 36 are provided on the exterior termination end for bonding to a second plurality of circuit traces (not shown) that may constitute part of the electronic package or an external circuit. The composition of the second solder bumps 36 is, independently, any one of those

specified for the first solder bump 34. Alternatively, the second solder bump may be formed on the second plurality of circuit traces in alignment with the exterior termination ends 32.

Figure 3 illustrates an electronic package 40 utilizing the component 20 as a cover component. The electronic package 40 includes a base component 42 that may be any desired material such as a metal, polymer or ceramic. Preferably, the base component 42 is also formed from a metal, metal alloy, metal composite or metal compound to take advantage of the high thermal conductivity of these materials. When electrically conductive, the base component 42 is coated with a non-conductive layer 44 as described above for the non-conductive layer 24.

The base component 42 has a centrally disposed integrated circuit device receiving portion 46 and a peripheral portion 48. Formed on the peripheral portion 48 is a second plurality of circuit traces 50 having characteristics similar to the first plurality of circuit traces 26.

An integrated circuit device 10 is bonded to the receiving portion 46 of the base component 42 by a die attach 52. The die attach 52 is any suitable low melting temperature solder, sealing glass or adhesive. One preferred material is an epoxy that is filled with a thermally conductive material such as silver powder. I/O pads 18 on the front side 12 of the integrated circuit device 10 are bonded to the first plurality of circuit traces 26 by the first bumps 34.

The second solder bumps 36 electrically interconnect the first plurality of circuit traces

26 to the second plurality of circuit traces 50. While the second solder bumps 36 bond the cover component 20 to the base component 42, to ensure tenacious adhesion, a polymer adhesive 54 is preferably employed to enhance the bond. This polymer adhesive 54 is any suitable material that bonds to both the non-conductive layers 24, 44 and to the conductive circuit traces 26, 50. One suitable material is a thermosetting epoxy.

The polymer adhesive 54 is bonded to a mid-portion of the second plurality of circuit traces 50. Bonded to an exterior portion 56 is a solder ball 58. The solder ball 58 is any suitable solder for joining the electronic package 40 to external circuitry and is typically a lead/tin alloy.

To minimize stress applied to the integrated circuit device 10 through the first solder bumps 34, the lid component 20 is preferably as thin as possible. Typically, the lid component 20 thickness is from about 0.13 mm to about 0.51 mm (0.005-0.02 inch). The thickness of the cover component 20 and the diameter of the solder balls 58 are selected so the solder balls 58 extend a distance, "D" of at least 0.13 mm (0.005 inch) and preferably from about 0.18 mm to about 0.25 mm (0.007-0.01 inch) above the outward facing surface of the cover component 20.

The electronic package 40 has many advantages over conventional ball grid array packages that utilize wire bond interconnections. The inductance is lower because the wire bonds are replaced with a buried microstrip structure. The lengths of the first circuit traces 26 are shorter than that of typical wire bonds because the circuit traces run

parallel to the surface of the semiconductor device 10 rather than running in an elevated arc as with wire bonding. Further, there is no problem with wire sweep and other issues related to wire fragility and the bond loop height is not a reliability concern. Bond loop height is significant in metal electronic packages because if the top of the arc contacts a metallic cover, an electrical short circuit develops. In addition, both the height and the shape of the bond wires affect wire reliability. This electronic package 40 is ideal for the removal of heat from the integrated circuit device 10. Both the metallic lid and the metallic base are directly connected to the device and constitute a dual heat sink. Further, the outward facing surface of the cover may be metallized for soldering to a printed circuit board.

With reference now to Figures 1 and 4, an electronic package 60 is formed by mechanically deforming the component 20 into a cup-shaped component 20'. The first plurality of conductive circuit traces 26 is formed on the metallic substrate 22. A non-conductive layer separates the first circuit traces 26 from the metallic substrate 22. Alternatively, the substrate 22 may be a heat formable plastic eliminating the need for the intervening non-conductive layer. Of course, thermal conductivity is enhanced when the substrate 22 is metallic.

The first circuit traces 26 are formed on the substrate 20 prior to deformation and are capable of being mechanically shaped without cracking. While an aluminum or aluminum alloy substrate with an

anodization layer is acceptable for this embodiment, it is preferred that the metallic substrate 22 be copper or a copper based alloy and that the non-conductive layer be a dielectric organic polymer, such as a polyimide or an epoxy. The dielectric layer is applied to the metallic substrate 26 by a suitable process such as dipping or spraying and has a thickness on the order of 0.025 mm to 0.075 mm (0.001-0.003 inch). If a polymer adhesive is required to laminate the circuit traces, an epoxy adhesive is suitable.

First bumps 34 electrically interconnect the I/O pads 18 to the interior termination ends 30 of the first circuit traces 26. The exterior termination ends 32 are electrically interconnected to a second plurality of circuit traces 50 by second solder bumps 36. The second plurality of circuit traces 50 may be formed on a base component or on a printed circuit board substrate 62 such as a glass filled epoxy resin.

The space between the front side 12 of the integrated circuit device 10 and the substrate 20 may be filled with a compliant polymer 64, such as a silicone gel, to enhance the reliability of the first bumps 34. Filling the entire package cavity with the compliant polymer enhances the reliability of the second solder bumps 36.

The advantages of the electronic package 60 include low cost and amenability to high volume manufacturing methods. Since the first plurality of conductive circuit traces 26 are deposited on a planar surface, high resolution of the circuitry is obtained. After deformation of the substrate 22,

the high density circuitry accurately fills the cupped region of the package. The depth of the cup may be accurately controlled during forming. As a result, a similar component 20 is used for many different sizes of integrated circuit devices by merely changing the deformation tool dimensions.

Figures 18 and 19 illustrate that the component 20 may be an internal component rather than a part of the package base or cover. The component 20 has a substrate 22, preferably a metal coated with a non-conductive layer 24. A plurality of integrated circuit devices 10, 10′ are bonded to opposing sides of the component 20. The back side 14 of the integrated circuit devices may be bonded to the component 20 and electrically interconnected through wire bonds 66 as illustrated in figure 18. The wire bonds connect the I/O pads 18 to the first plurality of circuit traces 26. The first circuit traces 26 provide electrical interconnection to external circuitry through solder balls, terminal pins, a lead frame or the like.

In Figure 19, the integrated circuit devices 10, 10′ are bonded and electrically interconnected to the first plurality of circuit traces 26 through first solder bumps 34. One or more conductive vias 68 may be included to electrically or thermally interconnect the devices.

The component 70 illustrated in cross-section in Figure 5 and in top planar view in Figure 6 provides hermeticity. Moisture is detrimental to the operation of an integrated circuit device. Moisture combines with byproducts of package assembly such as chloride ions to form corrosive

species that corrode circuitry on the integrated circuit device and the bond wires. Electronic packages that are hermetic effectively block the transfer of moisture to the integrated circuit device and bond wires.

The component 70 has a metallic substrate 72 coated with a non-conductive layer 74. The metallic substrate is any suitable metal, metal alloy, metal composite or metal compound, preferably aluminum or an aluminum alloy with the non-conductive layer 74 an anodization layer. Alternatively, the substrate 72 may be a dielectric such as a ceramic, for example, aluminum oxide, aluminum nitride or silicon carbide. When a dielectric substrate is employed, the non-conductive layer may be omitted.

A first plurality of circuitry traces 76 is formed on a peripheral surface 78 by any suitable process such as chemical vapor deposition, physical vapor deposition or jet vapor deposition. Alternatively, the circuit traces 76 may be formed by an electroless or electrolytic plating process.

The circuit traces 76 have an interior end 80, an opposing exterior end 82 and an intervening mid-portion 84. A dielectric layer 86 is formed over the mid-portion 84 of the circuit traces 76 by a vapor deposition process such as plasma vapor deposition or jet vapor deposition. This dielectric layer may be any suitable inorganic dielectric such as aluminum oxide or aluminum nitride.

A metallization layer 88 is deposited on the dielectric layer 86 by a suitable process such as vapor deposition. The metallization layer 88 is any solderable metal such as a palladium/nickel alloy or

nickel. A ceramic or metallic lid may then be joined to the component 70 by soldering or glass sealing. Solder balls 58 are available for electrical interconnection to external circuitry. However, other means for electrical interconnection through the exterior ends, such as brazed leads or terminal pins, may also be employed.

Another hermetic electronic package 90 is illustrated in cross-section in Figure 7. The base component 92 to the package 90 is shown in top planar view in Figure 8. As described hereinabove, the base component 92 is preferably a metallic substrate and coated with a non-conductive layer 93. A first plurality of circuitry traces 26 are formed about a peripheral surface 78 of the base component 92. Wire bonds 94, thin strips of copper foil as utilized in tape automated bonding (TAB), in-line circuitry or any other electrical interconnection connects the I/O pads 18 to the interior end 80 of the first plurality of conductive circuit traces 26.

The cover component 96 is bonded to the base component 92 by a sealing glass 98. The sealing glass 98 bonds to a peripheral surface 100 of the cover component 96 and to the mid-portion 84 of the first plurality of conductive circuit traces 26, as well as to the dielectric layer 94, if present or else to the substrate 92 if the substrate 92 is non-conductive.

When the substrate 92 is aluminum or an aluminum based alloy, one suitable sealing glass has the composition, by weight:

32%-50% SiO_2
4%-27% Na_2O
4%-27% K_2O

2%-8% BaO
2%-8% SrO
4%-30% TiO_2
up to 5% Li_2O
up to 7% ZnO
up to 2% ZrO_2
up to 2% Al_2O_3

as disclosed in U.S. Patent No.5,023,398 to Mahulikar et al. In addition to sealing glasses, devitrifying ceramics and ceramizable sealing glasses may also be employed.

A hermetic electronic package 110 is illustrated in cross-section in Figure 9. As with preceding embodiments, the hermetic electronic package 110 includes a base component 112 and a cover component 114, both of which are preferably a metal, metal alloy, metal composite or metal compound and coated with a non-conductive layer 116. Preferably, the base component 112 and cover component 114 are formed from aluminum or an aluminum alloy and the non-conductive layer 116 is an anodization layer. Optionally, either the base component 112 or the cover component 114 or both, may be formed from an electrically non-conductive material such as a ceramic or a polymer resin, eliminating the need for the non-conductive layer 116.

A plurality of vias 118 are formed through either the base component 112 or the cover component 114. A first plurality of conductive circuit traces 26 are formed on a surface 120 of either the base component 112 or the cover component 114. The first plurality of circuit traces extend along the walls of the vias 118 to an opposing surface 122 of either the base component 112 or the cover component 114.

An integrated circuit device 10 is electrically interconnected to the first plurality of circuitry traces by any suitable means as described above, for example, wire bonds, TAB or in-line circuitry.

In one embodiment, the vias 118 are then filled with a solder paste 124 that is heated to reflow forming a solid plug that seals the via 118. A solder ball 58 is bonded to the first circuit traces on the opposing surface 122.

Alternatively, a terminal pin 126 extends through the via 118 and is joined to the first circuit traces 26 by solder 124. The solder extends along the shank of the terminal pin 126 through the via 118 to provide a hermetic seal.

A peripheral portion 128 of both the base component 112 and the cover component 114 is coated with a metallization 130 of a solderable material such as copper or a copper/nickel alloy. A solder seal 132 hermetically joins the base component 112 to the cover component 114, completing the package 110.

If the base component 112 has side walls 134 or a brazed ring frame (not shown), the terminal pins 126 may extend outward, in generally planar orientation with the base and cover components as illustrated in Figure 10. As with the preceding embodiments, first circuit traces 26 electrically interconnect the integrated circuit device 10 to the terminal pins 126.

The solder 124 used to fill the vias 118 in Figures 9 and 10 may be either the same or different than the solder seal 132 used to join the base component 112 to the cover component 114. If the

same solder is used, then the lid attach and via filling operations are done at the same time.

If a sequential process is desired, then the solder 124 should have a higher melting point than the solder seal 132 recognizing that the solder seal 132 is the last assembly operation. Alternatively, the solder seal 132 may be replaced with a sequential localized heat seam sealing operation to prevent any melting of other solder joints in the package. This process limits the heat applied to a very local localized portion of the peripheral portion 128 of the package components.

The electronic package components of the invention are highly effective to dissipate heat from an integrated circuit device. The dissipation of heat may be further enhanced by forming a heat sink integral with either the base component, the cover component or both. One such component is illustrated in cross-sectional representation in Figure 11 and in top planar view in Figure 12. The thermally enhanced component 140 has a first surface 142 and an opposing second surface 144. An integrated circuit device 10 is bonded to the first surface 142. A plurality of protrusions 146 extend outward from the periphery of the second surface 144 to a height of from about 1 mm to about 25 mm. A central portion 148 of the second surface 144 is essentially free of the protrusions 146 or the protrusions may extend through the central portion in a waffle-like pattern as illustrated in Figure 22. A forced air draft 150 travels across the second surface 144 in a direction generally perpendicular to the rows of protrusions 146. The

configuration with the central portion free of protrusion is superior to fins extending all the way across the second surface 144 because the central portion 148 is then used for marking or pick and place.

A second thermally enhanced component 160 is shown in cross-sectional representation in Figure 13 and in top planar view in Figure 14. This structure is similar to the thermally enhanced component 140 of Figures 11 and 12 except that the protrusions 146′ extend outward from a central portion 162 of the second surface 144 and then extend generally parallel to the second surface.

A thermally enhanced electronic package 170 is illustrated in cross-section in Figure 15. The package 170 has a base component 172 and a cover component 174 both formed from any desired metal, ceramic or polymer. Preferably, metallic components are employed and most preferably the metallic components are aluminum or an aluminum based alloy coated with a non-conductive anodization layer as described hereinabove. The base component 172 is bonded to the cover component 174 by a sealant 176. The sealant 176 is any effective means of joining the base 172 to the cover 174 such as a polymer adhesive, for example, a thermosetting epoxy, or a metallic solder.

An integrated circuit device 10 is encapsulated within a cavity 178 defined by the combination of the base component 172 and cover component 174. Electrical interconnection of the integrated circuit device to external circuitry is by any means described hereinabove, for example, first solder

bumps 34 leading to a first plurality of conductive circuit traces (not shown) or a leadframe as illustrated in Figure 16.

With reference back to Figure 15, the base component, that component to which the back side 14 of the integrated circuit device 10 is bonded, contains at least one, and preferably a plurality, of apertures 180 that extend through the base component 172. A heat sink 182 formed from a thermally conductive material such as copper or aluminum and preferably having a black color to maximize emissivity, is bonded to the base component 172 by a sealant 184. This sealant may be any suitable adhesive, sealing glass or metallic solder. The remainder of the cavity 178 is then filled with a thermally conductive, electrically non-conductive fluid 186, such as perfluorinated heat transfer fluid.

As the integrated circuit device is powered by electrical signals, heat is generated. This heat is transferred into the fluid 186, causing a portion of the fluid to vaporize. The fluid vapors pass through the aperture 180 and enter the heat sink where the vapors condense and flow back into the cavity 178 establishing a heat pump.

With reference to Figure 16, the thermally enhanced electronic package 190 illustrates the applicability of the heat sink 182 bonded to the cover component 174 rather than the base component 172.

The thermal dissipation of the electronic packages of the invention is further enhanced by thermally coupling the package components and an

external heat sink. As illustrated in Figure 20, the package 40 of Figure 3 is thermally coupled to a printed circuit board 192 or other external substrate by forming a bond 194 between the component 20 and the printed circuit board 192. The bond 194 is a metallic solder, silver filled epoxy, thermal grease or any other suitable high thermal conductivity adhesive.

Thermal vias 196, such as copper filled through holes, may contact the component 20 to further enhance thermal dissipation. In the package 60, as illustrated in Figure 4, and other packages having the back side 14 of the integrated circuit device exposed to external components, the thermal vias 196 may be directly coupled to the back side 14 by a solder, thermally conductive adhesive or thermal grease. If a solder is employed, the back side 14 is appropriately metallized to enhance the solder bond

The electronic package 200 illustrated in Figure 21 is drawn to an embodiment in which the integrated circuit device 10 is electrically coupled to a metallic base component 42. The metallic base component 42 is coated with an electrically non-conductive layer 44 as described above. The electrically non-conductive layer 44 is discontinuous and has gaps 202 disposed between the metallic base component and a portion of the first plurality of circuit traces 26′ and a portion of the second plurality of circuit traces 50′. The gaps 202 are formed by mechanical or chemical removal or laser ablation of desired portion of the non-conductive layer 44. Alternatively, the selected

portions of the metallic base component 42 are masked or otherwise prevented from receiving the non-conductive layer 44. When the first and second circuit traces 26′ 50′ are deposited, the circuit traces fill the gap electrically coupling selected circuit traces 26′, 50′ to the metallic base component 42. Other circuit traces 26, 50 are electrically isolated from the metallic base component 42 by an underlying portion of the non-conductive layer 44.

Selected I/O pads 18′ of the integrated circuit device 10 are electrically interconnected to the first plurality of circuit traces 26′ by wire bonds 94, in-line circuitry as described above, TAB bonding or any other suitable method.

While the package base 42 may constitute a floating ground, preferably, the second circuit traces 50′ are electrically interconnected to an external ground. Any circuit trace location may be electrically coupled to the metallic base. Preferably, the coupled first circuit trace 26′ and the coupled second circuit trace 50′ are widely separated, such as being disposed on opposing sides of the integrated circuit device 10. In this manner, the ground current flows over a large area of the metallic base component leading to the following benefits:

1. There is a better distribution of current flow and lower resistance than if the ground plane was fashioned from many small individual circuit traces or wires.

2. The package "noise" is reduced, particularly at high frequencies. The voltage noise

associated with ground return paths, referred to as "ground bounce" is defined by:

$$V_{noise} = L(di/dt)$$

where (di/dt) is the speed of the circuit

L is the circuit inductance

The electrically coupled circuit of the invention reduces circuit inductance resulting in reduced package noise.

While particularly drawn to ball grid array packages, the packages of the invention are equally applicable to pin grid array packages, leaded packages and lead less packages. For example, leads could be soldered to the exterior termination ends of the first plurality of circuit traces.

It is apparent that there has been provided in accordance with the present invention electronic package components particularly suited for ball grid array electronic packages that fully satisfy the objects, means and advantages set forth hereinabove. While the invention has been described in combination with embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, it is intended to embrace all such alternatives, modifications and variations as fall within the spirit and broad scope of the appended claims.

IN THE CLAIMS:

1. A component (20, 20′) for an electronic package (40) characterized by:

a metallic substrate (22) coated with a flexible dielectric polymer layer (24); and

a first plurality of conductive circuit traces (26) formed on a surface (28) of said flexible dielectric polymer layer (24), said first plurality of circuit traces (26) bonded (34) directly to the input/output pads (18) of an integrated circuit device (10) and to a second plurality of circuit traces (50).

2. The component (20, 20′) of claim 1 characterized in that said flexible dielectric polymer layer (24) is an epoxy.

3. The component (20, 20′) of claim 1 characterized in that said first plurality of circuit traces (26) are bonded to said input/output pads (18) by a material (34) selected from the group consisting of metals, metal alloys, conductive solder glasses, conductive polymers and solder coated metallic balls.

4. The component (20′) of either claim 1, 2 or 3 characterized in that said component (20′) has a generally cup-shaped configuration with said integrated circuit device (10) housed within said cup.

5. The component of claim 4 characterized in that a compliant polymer (64) is disposed between said integrated circuit device (10) and said component (20').

6. A component (20) for an electronic package characterized by:

a metallic substrate (22) coated with an electricallly non-conductive layer (24);

a first plurality of conductive circuit traces (26) formed on opposing surfaces of said metallic substrate (22), said first plurality of circuit traces (26) bonded (66) directly to the input/output pads of at least two integrated circuit devices (10, 10') bonded to opposing surfaces of said metallic substrate (22) and to a second plurality of circuit traces; and

a via (68) extending through said metallic substrate (22) between at least two of said integrated circuit devices (10, 10').

7. A component (20) for an electronic package characterized by:

a metallic substrate (22) coated with an electrically non-conductive layer (24);

at least two integrated circuit devices (10, 10') bonded to opposing surfaces of said metallic substrate (22); and

a first plurality of conductive circuit traces (26) formed on opposing surfaces of said metallic substrate (22) wherein the input/output pads of said at least two integrated circuit devices are directly soldered (34) to said first plurality

of circuit traces (26), said first plurality of circuit traces (26) further bonded to a second plurality of circuit traces.

8. A package (40) for housing an integrated circuit device (10) characterized by:

a metallic cover component (20) coated with an electrically non-conductive layer (24) and having a first plurality of circuit traces (26) formed on a surface thereon;

a base component (42) having an integrated circuit device (10) receiving portion (46) and a peripheral portion (48), said peripheral portion (48) having a second plurality of circuit traces (50) formed thereon;

said integrated circuit device (10) bonded (52) to said receiving portion (46) and soldered (34) to said first plurality of circuit traces (26) by a first solder joint (34);

a second solder joint (36) electrically interconnecting said first plurality of circuit traces (26) to said second plurality of circuit traces (50); and

a third solder joint (58) electrically interconnecting said second plurality of circuit traces (50) to an external circuit.

9. The package (40) of claim 8 characterized in that said metallic cover component (20) is aluminum or an aluminum alloy and said electrically non-conductive layer (24) is an anodic film.

10. The package (40) of claim 8 characterized in that said electrically non-conductive layer (24) is selected from the group consisting of carbides, nitrides, oxides and dielectric polymers.

11. The package (40) of either claim 8, 9 or 10 characterized in that said third solder joint (58) constitutes solder balls extending beyond an outward facing surface of said cover component (20).

12. The package (40) of anyone of claims 8, 9, 10 or 11 characterized in that said cover component (20) is thermally coupled to an external heat sink.

13. The package (40) of claim 12 characterized in that said external heat sink is a printed circuit board (192) containing at least one thermally conductive via (196) extending from said cover component (20).

14. The package (40) of claim 12 characterized in that said external heat sink (182) has an internal channel that delivers a thermal fluid (178) to said package.

15. The package (40) of claim 12 characterized in that said base component (42) contains a plurality of integral protrusions (146) extending

outwardly from the periphery of said base and a central portion (148) that is essentially free of said protrusions (146).

16. The package (40) of claim 12 characterized in that said base component (42) contains a plurality of protrusions (146′) extending outwardly from said base component (42) and running generally parallel to a major surface (144) of said base component (42).

17. The package (40) of anyone of claims 8-11 characterized in that said base component (42) is also metallic and a portion (26′) of said first plurality of circuit traces (26) is electrically coupled (202) to said metallic base component (42).

18. A component (70) for an electronic package characterized by:

a metallic substrate (72) coated with a first electrically non-conductive layer (74);

a first plurality of conductive circuit traces (76) formed on a peripheral surface (78) of said metallic substrate, said first plurality of circuit traces (76) having an interior end (80), an exterior end (82) and an intervening mid-portion (84); and

a second electrically non-conductive layer (86) formed about the periphery of said metallic substrate (72) overlying said mid-portion (84) of said first plurality of cirucit traces 76.

19. The component (70) of claim 18 characterized in that said metallic substrate (72) is an aluminum or aluminum alloy coated with an anodic film (74).

20. The component (70) of claim 18 or 19 characterized in that said second electrically non-conductive layer (86) is selected from the group consisting of aluminum oxide and aluminum nitride.

21. The component (70) of claim 20 characterized in that a metallized layer (88) is disposed on a side of said second electrically non-conductive layer (86) opposite said intervening mid-portion (84).

22. The component (70) of claim 21 characterized in that said metallized layer (88) is

selected from the group consisting of palladium/nickel alloys, molybdenum/manganese alloys, nickel and nickel alloys.

23. A component for an electronic package characterized by:

a metallic substrate (112) coated with an electrically non-conductive layer (116) and having a plurality of vias (118) extending therethrough;

a first plurality of conductive circuit traces (26) formed on a surface of said metallic substrate (112) and extending through said plurality of vias (118); and

an electrical contact (124) disposed within said plurality of vias (118) and electrically interconnected to said first plurality of circuit traces (26).

24. The component of claim 23 characterized in that said electrical contact (124) is a solder plug.

25. The component of claim 23 characterized in that said electrical contact is a terminal pin (126) extending perpendicular to a major surface (120, 122) of said metallic substrate (112).

26. The component of claim 23 characterized in that said electrical contact is a terminal pin (126) extending parallel to a major surface (120, 122) of said metallic substrate (112).

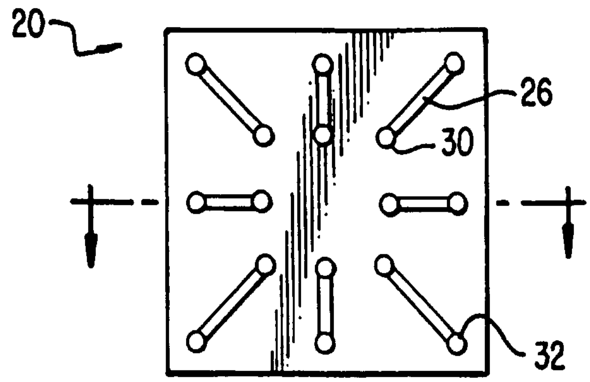

FIG. 1

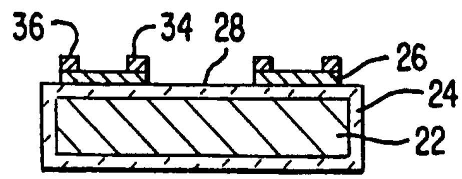

FIG. 2

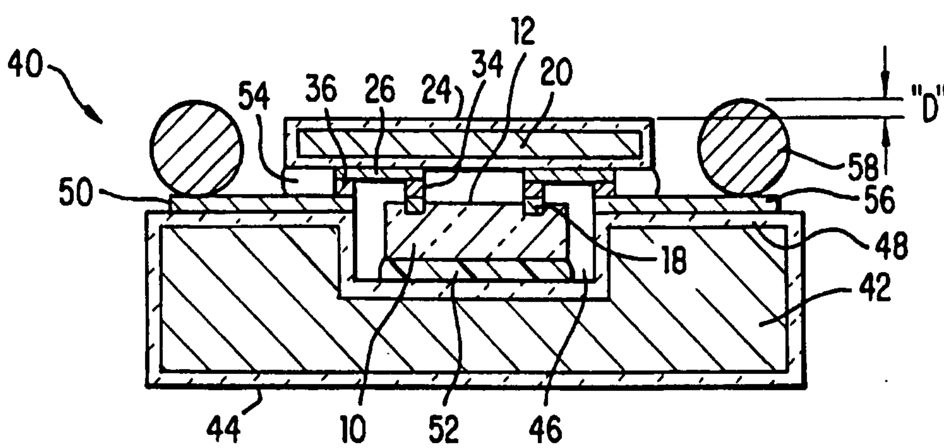

FIG. 3

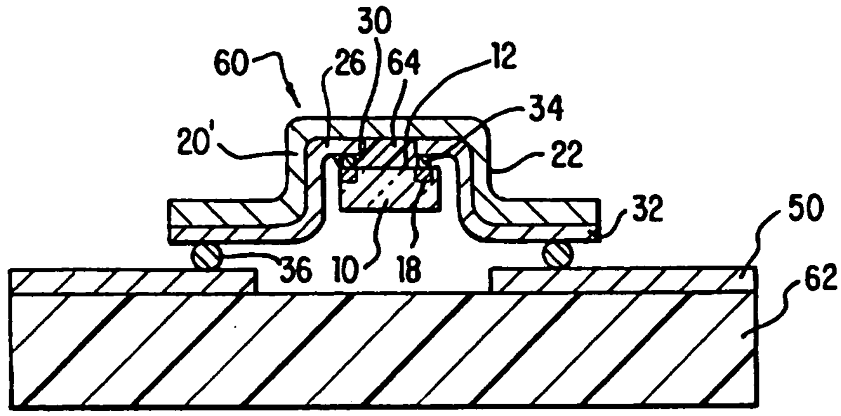

FIG.4

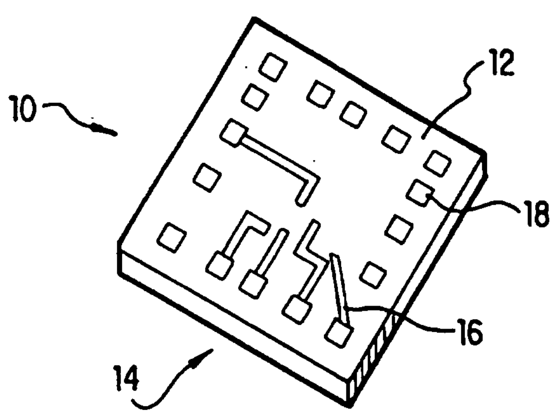

FIG.17 PRIOR ART

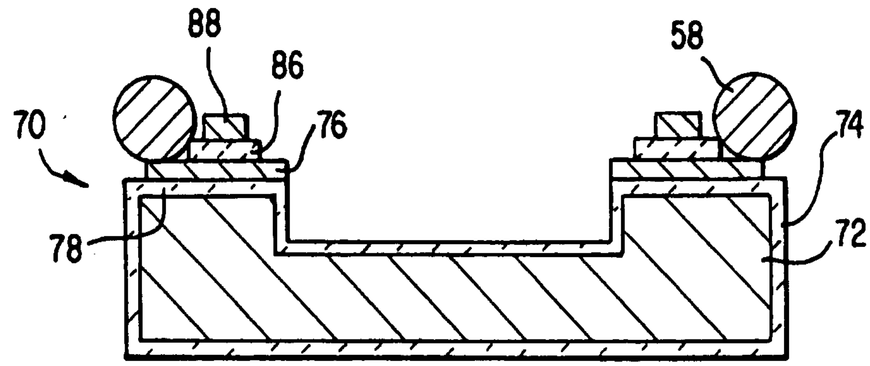

FIG. 5

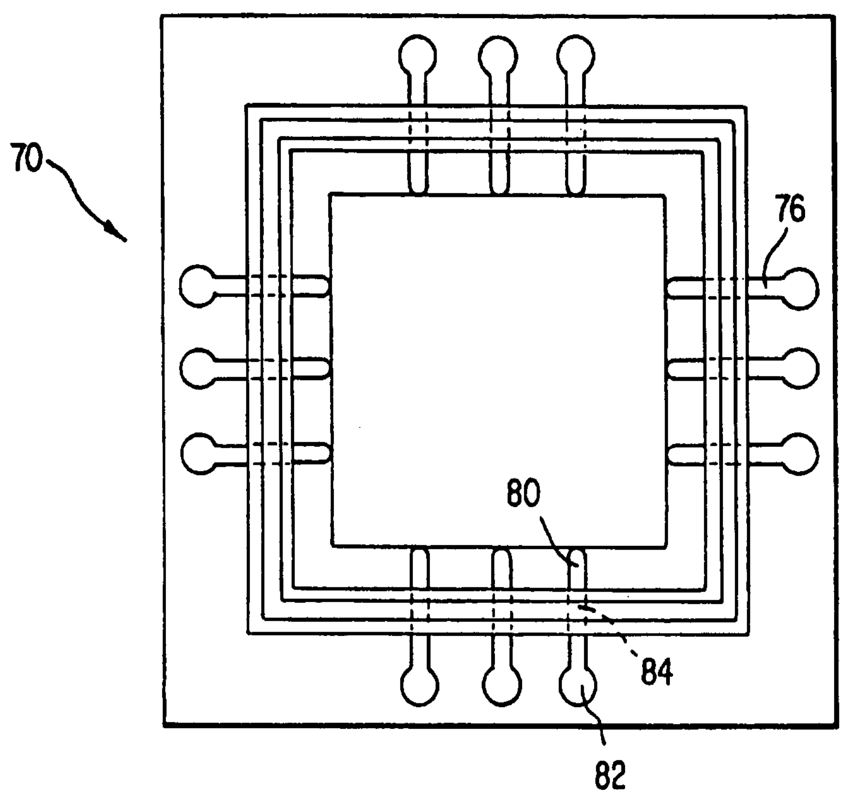

FIG. 6

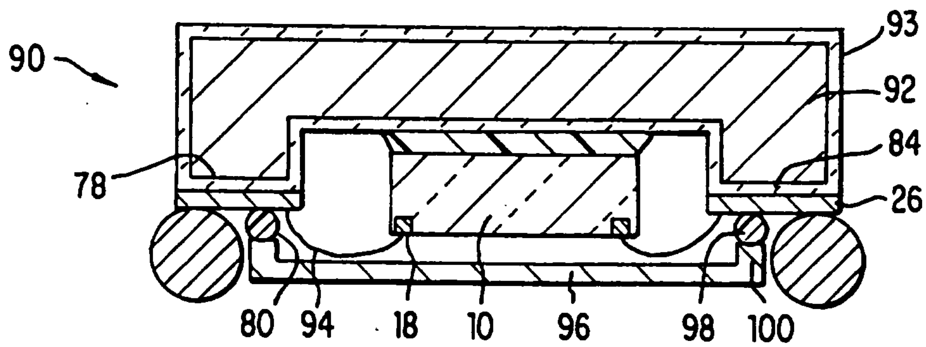

FIG.7

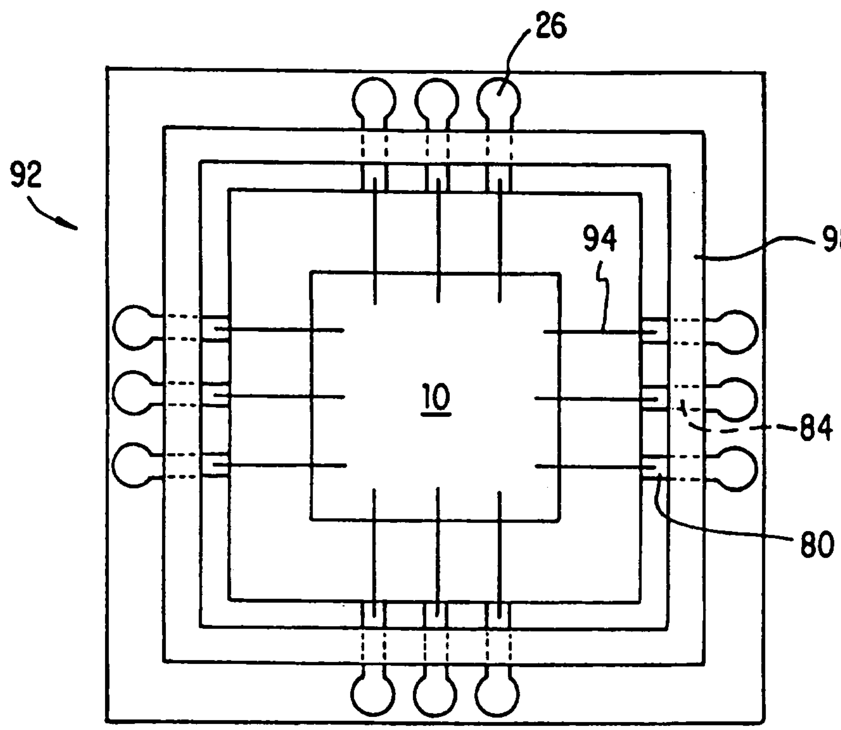

FIG.8

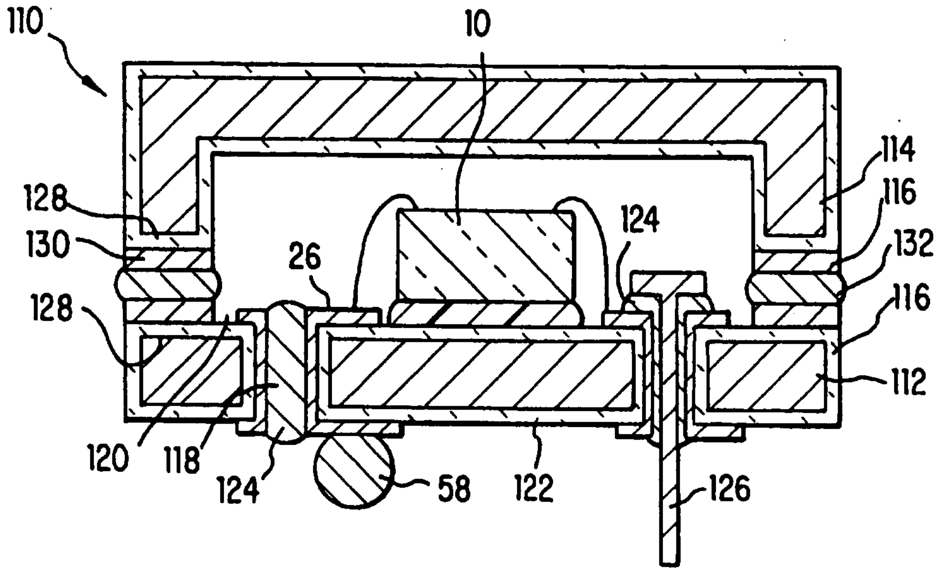
110
10
114
116
128
124
130
132
26
128
116
112
120
118
124
58
122
126

FIG. 9

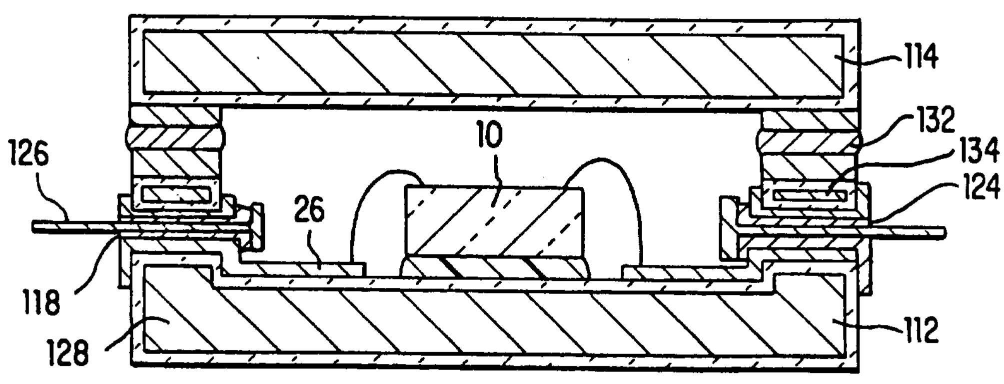
114
132
10
134
126
124
26
118
112
128

FIG. 10

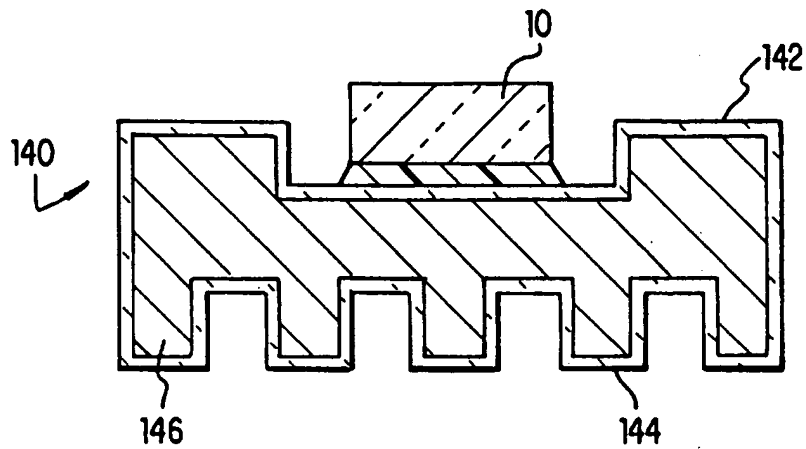

FIG. 11

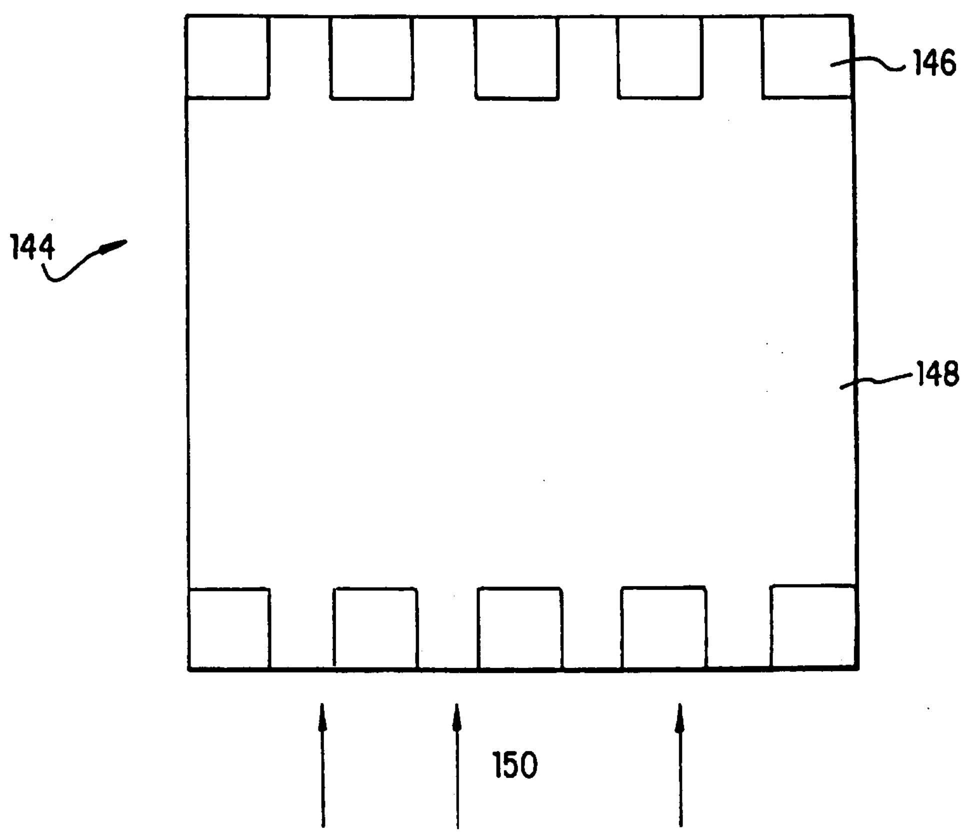

FIG. 12

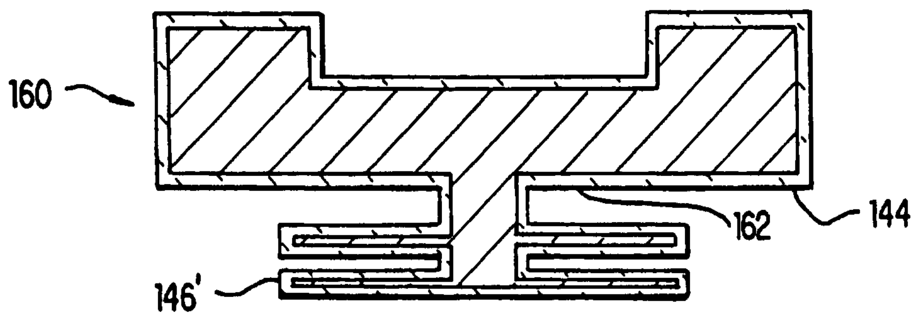

FIG. 13

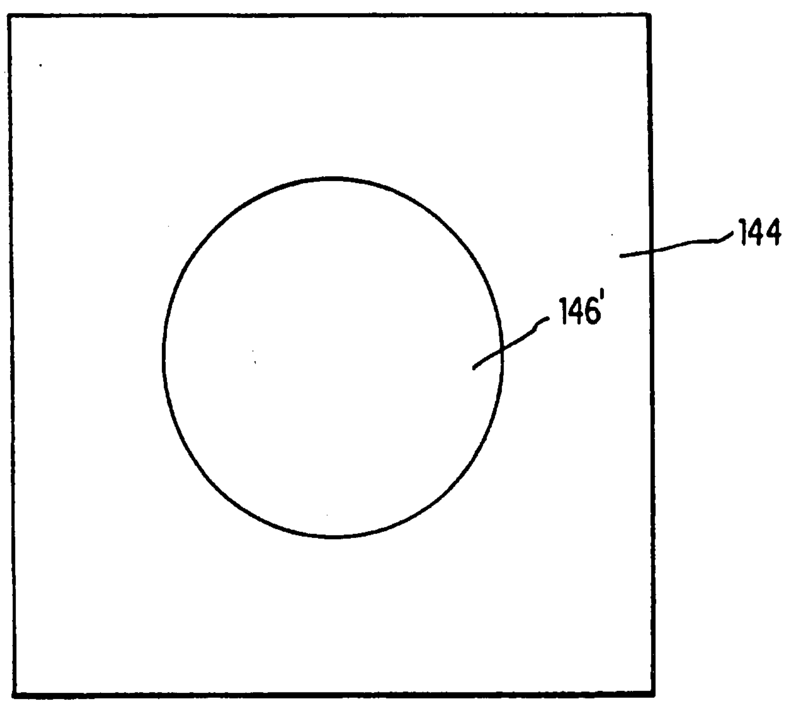

FIG. 14

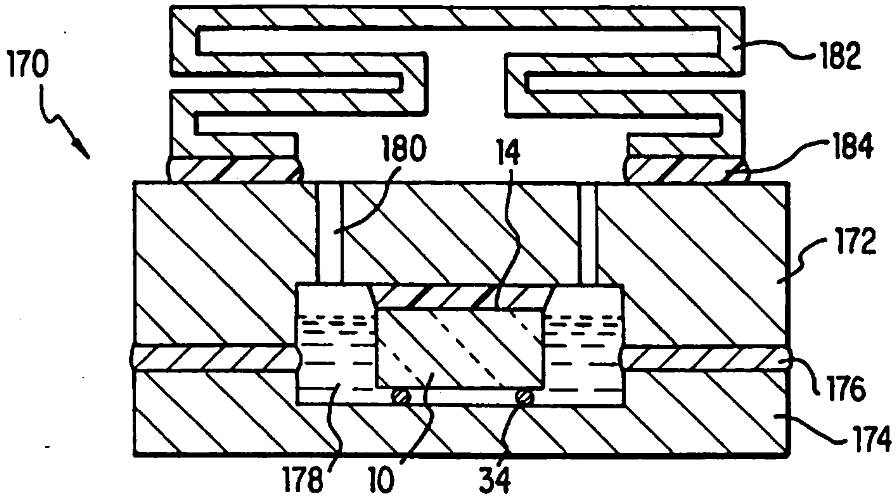

FIG. 15

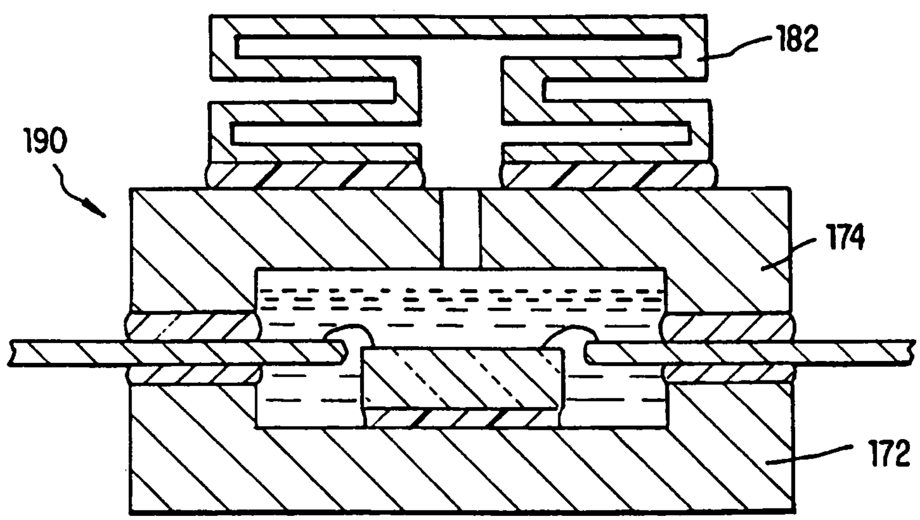

FIG. 16

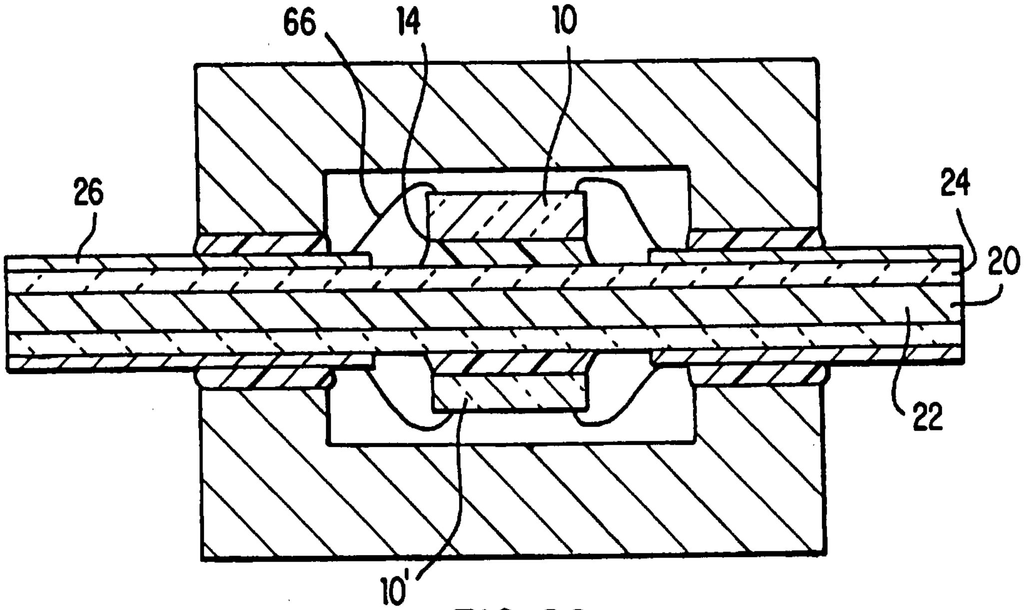

FIG. 18

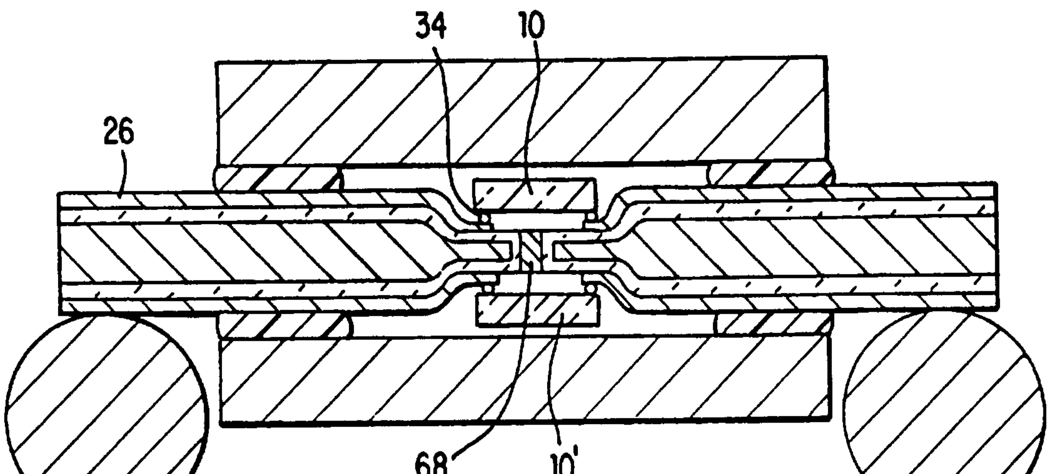

FIG. 19

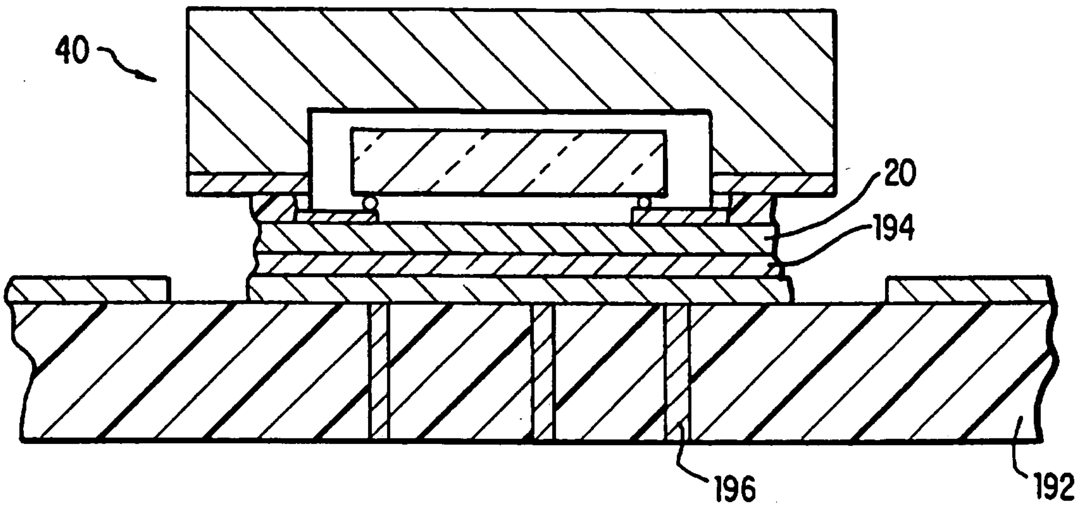

FIG. 20

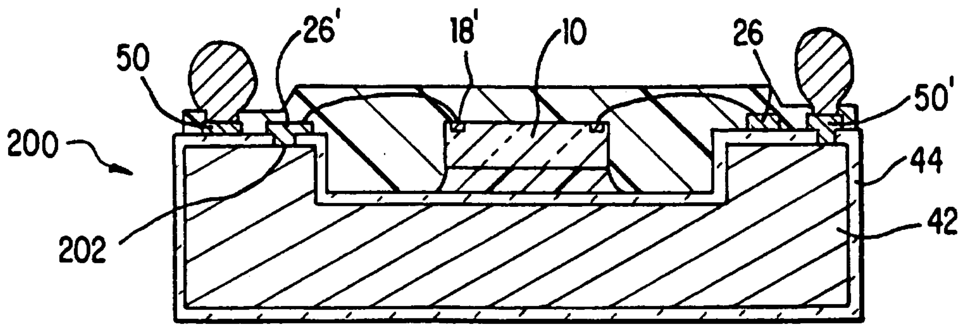

FIG. 21

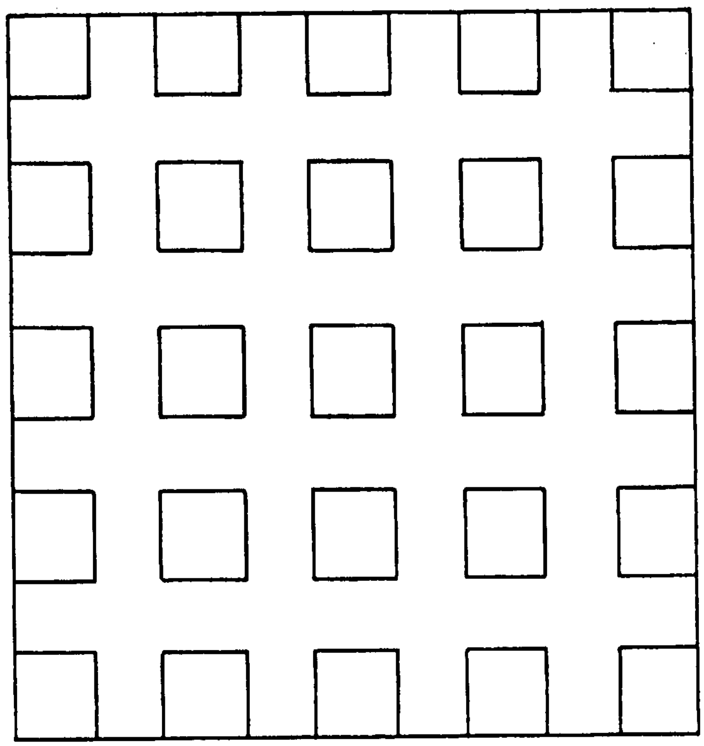

FIG. 22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/03258

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :HO1L 23/02. 23/10. 23/29. 23/48. 23/49. 23/52. 23/34. 29/40.
US CL : 257/675,676,678,684,697,698,704,706,712,717,720,771,772,783.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/675,676,678,684,697,698,704,706,712,717,720,771,772,782.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

IMAGE SEARCH, APS.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,968,552, (Linde), 06, November, 1990, column 25-32.	1, 2,6-8, 10, 18, 23
Y	US, A, 4,806,503, (Yoshida et al.), 21 February, 1989, Figures 1a-1c.	3
Y	US, A, 4,888,449, (Crane et al.), 19 December 1989, column 3, lines 24-30.	5
Y	JP, A, 4-216655, (Kimura), 08 June, 1992, Figure 1.	6 and 7
Y	US, A, 4,939,316, (Muhulikar et al.), 03 July, 1990, Figure 1, column 3, line 16.	4, 9, 19.
Y	JP, A, 60-136348, (Sawara), 19 July, 1985, Figures 1 and 2.	12-16.

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier document published on or after the international filing date	
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 JULY 1996	25 JUL 1996

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	JHIHAN B. CLARK
Facsimile No. (703) 305-3230	Telephone No. (703) 308-4857

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/03258

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,897,508, (Muhulikar et al.) 30 January, 1990, Figure 1.	17
Y	JP, A, 2-60149, (Tsujimoto et al.), 28 February, 1990, Figure 1 or 5 or 6 or 7.	11, 16-26.
Y, P	US, A, 5,352,926, (Andrews), 04 October, 1994 Figure 1.	3

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